
**Intellectual Property Prosecution, Transactions & Portfolio Management Update**

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# Contrasting PTAB Analyses of Patent Eligibility in Recent Semiconductor Cases

## Introduction

Two recent decisions from the Patent Trial and Appeal Board (PTAB) at the U.S. Patent and Trademark Office (USPTO) illustrate the divergent outcomes that can arise under the same Section 101 eligibility framework, depending on how the Board characterizes the claims at issue. In *Ex parte Lei* (Appeal 2025-000504), the Board affirmed the Examiner's Section 101 rejection of claims directed to a semiconductor circuit layout method, finding them directed to abstract mental processes without an inventive concept. In contrast, *Ex parte Pisarenco* (Appeal 2025-003305) resulted in a reversal of the Examiner's Section 101 rejection, with the Board finding that claims directed to detecting defects in printed semiconductor patterns were not abstract ideas because the claimed steps could not be performed in the human mind.

This alert highlights the key analytical differences between these two decisions and offers guidance for patent applicants navigating Section 101 rejections in the semiconductor and electronic design automation fields.

## The Alice/Mayo Framework Applied

Both decisions applied the USPTO's 2019 Revised Patent Subject Matter Eligibility Guidance, as incorporated into MPEP Section 2106. Under this framework, examiners first determine whether the claim recites a judicial exception (Step 2A, Prong 1), then evaluate whether any additional elements integrate the exception into a practical application (Step 2A, Prong 2) and finally assess whether the claim adds an inventive concept beyond the judicial exception (Step 2B).

## Step 2A, Prong 1: Identifying an Abstract Idea

The critical divergence between these two decisions occurred at Step 2A, Prong 1, where the Board determines whether the claims recite a judicial exception, such as a mental process.

In *Ex parte Lei*, the Board agreed with the Examiner that certain claim limitations, namely identifying transistors in a circuit, determining that two transistors satisfy a merging priority, and combining active regions to form a mega transistor, constitute mental processes. The Board rejected the Appellant's argument that the human mind is "not configured to" perform these operations, finding instead that "[l]ooking at a schematic and determining whether two transistors have a common active region is something that can be performed in the human mind." The Board further noted that the use of a "standard cell layout application" to execute these steps did not change the analysis, because "claims can recite a mental process even if they are claimed as being performed on a computer."

Critically, the Board in *Ex Parte Lei* emphasized that Step 2A, Prong 1 requires examiners to identify specific limitations that recite abstract ideas, not merely to show that every limitation does so. Thus, the presence of some non-abstract limitations (such as "fabricating a semiconductor device") did not prevent a finding that the claim as a whole recites a judicial exception.

In *Ex parte Pisarenco*, the Board reached the opposite conclusion. The Examiner had characterized the "determining" and "improving" limitations in the claims as mental processes. However, the Board disagreed, holding that "determining the existence of a defect in a printed pattern on a semiconductor substrate based on a generated combined image is not an abstract idea because it cannot be performed in the human mind." The Board reasoned that "[t]he size of semiconductor substrates would make it impossible for a human to visually locate defects and mentally improve upon them."

Because the Board found no abstract idea at Step 2A, Prong 1, it did not proceed to analyze Step 2A, Prong 2, or Step 2B, and instead reversed the rejection outright.

## Step 2A, Prong 2: Practical Application

In *Ex Parte Lei*, having found that the claims recite a mental process, the Board proceeded to evaluate whether additional elements integrate the judicial exception into a practical application. The Appellant argued that the claims "recite a technical improvement to the technological field of circuit layout and fabrication." The Board was not persuaded. It noted that the Appellant's arguments relied on disclosures in the Specification about standard cell layout applications, fabrication tools, and masks, but that claim 1 "does not recite masks or their use in fabricating a circuit."

The Appellant also invoked the machine-or-transformation test, arguing that "fabricating a semiconductor device comprising the circuit" transforms an article to a different state. The Board rejected this argument, finding that the claim does not recite a wafer or the transformation of a wafer into an integrated circuit. The arguments were therefore "not commensurate in scope with the claimed subject matter."

## Step 2B: Inventive Concept

In *Ex Parte Lei*, the Board found that the additional claim elements did not contribute an "inventive concept" sufficient to transform the abstract idea into patent-eligible subject matter. The Appellant argued that the claims provide an improvement to semiconductor production that reduces energy consumption and enhances circuit performance. However, the Board held that the Appellant "does not address, let alone rebut, the Examiner's findings that fabricating a semiconductor device, using standard cell libraries, and merging active layers of transistors are conventional." During prosecution, the Examiner had cited prior art references demonstrating the conventionality of these techniques.

The Appellant's conclusory assertion in the Reply Brief that "fabrication of semiconductor devices including merged active areas according to the present claims are neither conventional nor routine" was insufficient to rebut the Examiner's findings. Accordingly, the Board sustained the Section 101 rejection.

## Practical Guidance for Applicants

These decisions highlight several strategies for patent applicants facing Section 101 rejections in the semiconductor and EDA fields.

First, applicants should emphasize claim limitations that cannot practically be performed in the human

mind due to the physical characteristics of the subject matter. The *Ex parte Pisarenco* decision demonstrates that pointing to physical constraints, such as the size of semiconductor substrates making visual inspection impossible, can be an effective way to avoid characterization as a mental process.

Second, applicants must ensure that their arguments are commensurate in scope with the actual claim language. In *Ex parte Lei*, the Board repeatedly faulted the Appellant for relying on Specification disclosures (such as masks and wafer transformation) that were not actually recited in the claims.

Third, when the Examiner cites prior art to demonstrate that additional claim elements are well-understood, routine, and conventional, applicants must directly rebut those findings with specific evidence or arguments. Conclusory denials of conventionality are insufficient.

## FOR MORE INFORMATION

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